WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor chip including an integrated circuit;

an interconnect electrically connected to the integrated circuit;

a pad that is a part of the interconnect and disposed on a front surface of the semiconductor chip;

wirings electrically connected to the pad;

an external terminal provided over and electrically connected to the wirings; and

a resin layer surrounding the external terminal and extending to a side face of the semiconductor chip.

2. The semiconductor device according to claim 1, wherein the semiconductor chip has a thin-wall part at edges thereof, and the resin layer extends to the thin-wall part.

3. The semiconductor device according to claim 2, wherein the semiconductor chip has a first face perpendicularly descending from the front surface, a second face perpendicularly ascending from a back surface opposite to the front surface, and a third face parallel to the front surface and connecting the first face with the second face, and the resin layer formed on the first face, but not on the second face.

4. The semiconductor device according to claim 2, wherein the semiconductor chip has a first face perpendicularly descending from the front surface, a second face perpendicularly ascending from a back surface opposite to the front surface, and a third face that curves to connect the first face with the

second face, and the resin layer is formed on the first face, but not on the second face.

5. The semiconductor device according to claim 3, wherein the resin layer is also formed on the third face.

6. The semiconductor device according to claim 2, wherein the semiconductor chip comprises a first face descending from the front surface and a second face ascending from a back surface opposite to the front surface, the first face and the second face being formed at different angles, and the resin layer formed on the first face, but not on the second face.

7. The semiconductor device according to claim 2, wherein the semiconductor chip comprises a first face curved in a descending manner from the front surface and a second face vertically ascending from a back surface opposite to the front surface, and the resin layer formed on the first face, but not on the second face.

8. The semiconductor device according to claim 1, further comprising a stress relaxation layer formed on the semiconductor chip, wherein the wirings are formed on the stress relaxation layer and the resin layer is formed over the stress relaxation layer.

9. The semiconductor device according to claim 1, further comprising a resist layer covering the wirings other than a region for providing the external terminal, wherein the resin layer is formed over the resist layer.

10. A circuit board on which a semiconductor device according to claim 1 is

mounted.

11. An electronic apparatus comprising a semiconductor device according to claim 1.

12. A semiconductor wafer, comprising:

a semiconductor substrate including a plurality of integrated circuits;

an interconnect electrically connected to each of the integrated circuits;

pads that are parts of the interconnect and disposed on a front surface of the semiconductor substrate, wherein grooves are formed in the front surface;

wirings electrically connected to the pads;

external terminals provided over and electrically connected to the wirings; and

a resin layer surrounding the external terminals and covering the grooves.

13. The semiconductor wafer according to claim 12, wherein the grooves surround each of the integrated circuits.

14. The semiconductor wafer according to claim 12, wherein a side face and a bottom face of each groove are connected via a curved surface.

15. The semiconductor wafer according to claim 12, wherein a face of each groove is inclined.

16. The semiconductor wafer according to claim 12, further comprising a stress relaxation layer formed on the semiconductor substrate, wherein the wirings are formed on the stress relaxation layer and the resin layer is formed over the stress relaxation layer.

17. The semiconductor wafer according to claim 12, further comprising a resist layer covering the wirings other than a region for providing the external terminals, wherein the resin layer is formed over the resist layer.

18. A method for manufacturing a semiconductor device, comprising:

(a) forming grooves in a front surface of a semiconductor substrate that includes a plurality of integrated circuits, an interconnect electrically connected to each of the integrated circuits, and a pad that is a part of the interconnect and disposed on the front surface of the semiconductor substrate;

(b) forming wirings so as to be electrically connected with the pad;

(c) providing an external terminal over the wiring so as to be electrically connected with the wirings;

(d) providing a resin layer so as to surround the external terminal and cover the grooves; and

(e) cutting the semiconductor substrate together with the resin layer in the grooves.

19. The method for manufacturing a semiconductor device according to claim 18, further comprising forming the grooves so as to surround each of the integrated circuits.

20. The method for manufacturing a semiconductor device according to claim 18, further comprising forming each of the grooves such that a side face and a bottom face of the grooves thereof are connected via a curved surface.

21. The method for manufacturing a semiconductor device according to claim 18, further comprising forming each of the grooves such that a side face thereof is inclined.

22. The method for manufacturing a semiconductor device according to claim 18, further comprising:

forming a stress relaxation layer on the semiconductor substrate before step (b);

forming the wirings on the stress relaxation layer in step (b); and

the resin layer forming over the stress relaxation layer in step (d).

23. The method for manufacturing a semiconductor device according to claim 18, further comprising:

forming a resist layer before step (c) so as to cover the wirings other than a region for providing the external terminal; and

forming the resin layer over the resist layer in step (d).